**Department of Electrical and Electronic Engineering**

2020 Third Year Industrial Group Project Brief

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| **Name of Company** | Intel |
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| **Introduction to Company** | Intel Programmable Solutions Group (PSG), formerly Altera, is the FPGA division of Intel. |
| **Project Description**  Describe the problem to be solved by the project team giving as much details as possible. | A common requirement of video processing systems is the ability to convert from one frame rate at the input to a different frame rate at the output (for example, converting 24fps film footage to 60fps for display on typical televisions).  The simplest method for converting frame rates is to drop or repeat input frames to produce the required output rate, but this can lead to undesirable judder in the output video which the human visual system is surprising good at detecting.  A less naïve approach is to try to create additional frames at points in time between two original input frames that correspond to the ideal sampling point for the output frame rate. So, for example, converting from 30fps to 60fps would require additional frames to be created at a time point that is halfway between each pair of input frames. Methods to do this generally involve some form of interpolation, but can also extend to include some form of motion estimation and scene change detection. This is generally accepted to be a hard problem to solve well, and it is easy to make the interpolated video look much worse than the results achieved through drop and repeat.  There is a great deal of existing literature on methods from interpolated frame rate conversions, but we have not had the time available to investigate this and evaluate   1. The video quality obtained through various algorithm 2. The relative (high level) costs of each algorithm in terms of block RAM usage and DDR bandwidth required   This project could be split into 3 phases:   1. Literature review to investigate existing algorithms 2. Software implementation of a small number of algorithms of interest (as few as one), evaluation of quality compared to golden results and drop/repeat. This can be done in a high level environment such as MATLAB. 3. Proposal of high level hardware architecture, possibly including estimation of block RAM usage and DDR bandwidth required   The students may not complete all three phases, and the phase 3 would be treated very much as a stretch goal, but any results produced would be of interest. |
| **Commercial/Industrial context** for project | We have requests for this feature from customers and would be interested in ultimately implementing a solution to productise and release. The hope would be that the output from this project could form the starting point for a full implementation |
| **Challenges** – technical and professional | From a technical point of view, this project would expose students to the full flow of developing algorithmic hardware for FPGAs. In the early stages of the project students will need to demonstrate good critical analysis. Later stages will encourage effective teamwork as the students will need to partition and implement complex algorithms, with each student implementing part of the portioned problem before the solution is integrated. |
| **Roles/Expertise/Skills required** i.e. any particular skills that would be essential/desirable | * Some experience with digital signal processing * Good software skills * Interest in digital systems and hardware implementation |
| **Resources** available:  £ in excess of £500  Personnel  Equipment | This project should not require any software or hardware resources beyond those available in the Imperial computer labs.  In terms of personnel, Intel can provide someone to act as an advisor, if required, with 1-2 hours per week available for advice, progress updates etc. via Skype and/or email. A day can also be set aside for an initial project kick-off meeting. |